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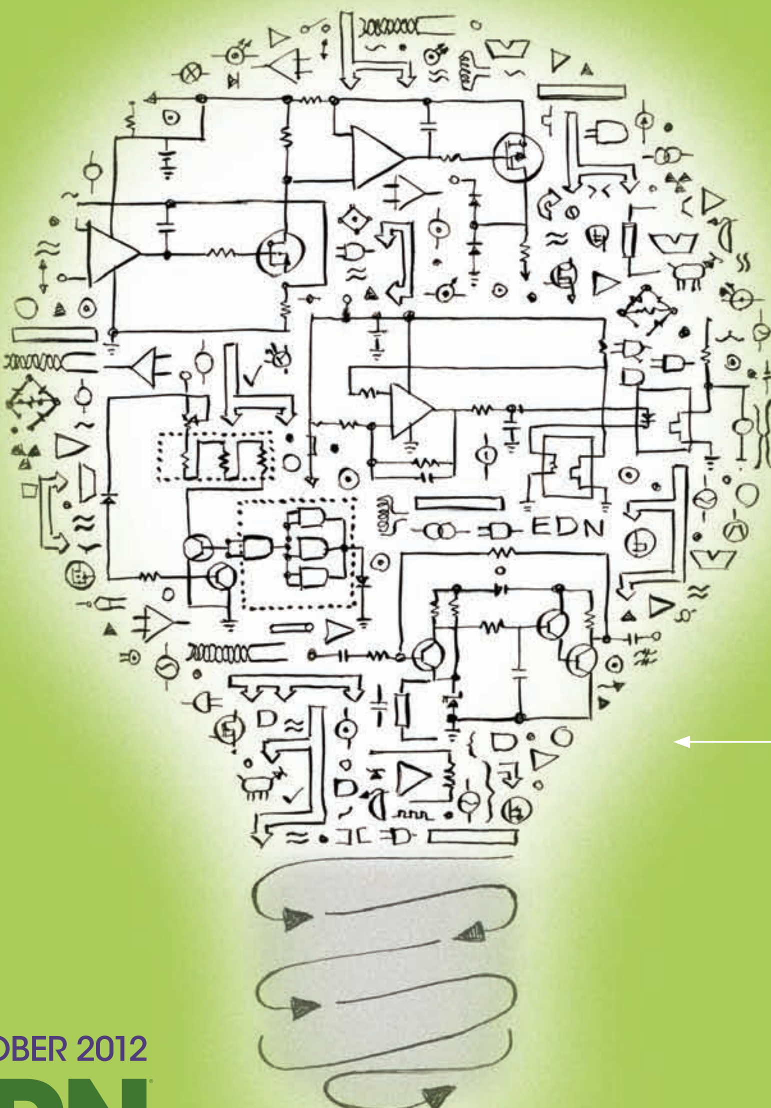

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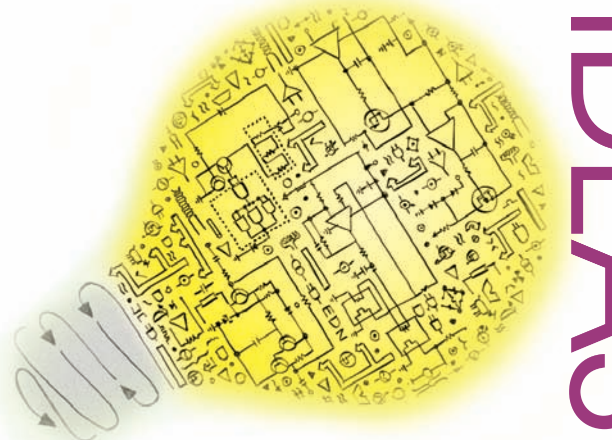

A SPECIAL SUPPLEMENT TO *EDN*

COVER IMAGE: DANIEL VASCONCELLOS

> "IDEAS ARE WHAT EVERY ENGINEERING ORGANIZATION HAS IN COMMON," OUR FIRST EDITOR, MILTON SOL KIVER, WROTE BACK IN 1956. HOW INTERESTING THAT, 56 YEARS LATER, ENGINEERS STILL HAVE THE SAME HUNGER FOR DESIGN IDEAS.

I recently had the opportunity to see *EDN*'s print archives. The vault area, housed in our Bedford, MA, office, stores original copies that date back to issue No. 1, published as *Electrical Design News* on May 8, 1956. I was six years old when *EDN* debuted.

As I sat down and leafed through the 122-page first edition, the first piece that caught my eye was the editorial by Milton Sol Kiver, the publication's first editor and the author of *Transistors in Radio, Television, and Electronics*, published by McGraw-Hill in 1959.

"We are beginning what we believe will be a helpful service to electrical design engineers," Kiver wrote. " 'What,' we asked, 'would you desire most to see in an electrical publication?' The response was as direct as it was unanimous … a magazine of design ideas."

The editorial continues: "No engineer, we found, can ever get enough good ideas. Ideas represent the most important piece of property in every engineering department, whether it be concerned with the evolution of fantastically complex and intricate computers or merely a simple, two-piece widget that sells for 18 cents. Ideas are what every engineering organization has in common—and will continue to have in common for as long as they remain in business."

The aim of *Electrical Design News*, Kiver wrote, was "to provide you with a maximum of ideas which will help you solve present or future problems or perhaps suggest methods of approach that were never even considered."

How interesting that, 56 years later, engineers still have the same need and hunger for Design Ideas. As the new Design Ideas editor, as well as a longtime *EDN* reader, I truly value their content. Ever since I graduated from New York University's School of Engineering in 1972, I have been tearing out Design Ideas and putting them in folders for near- or far-term use as references for my designs.

Design Ideas—community driven, and offering inspired, hands-on, practical, useful circuit-design contributions—have always resonated deeply with *EDN*'s audience. To highlight those contributions, and the engineers behind them, we collected the most popular Design Ideas published since January 2011 in six categories—Analog, Components and Packaging, LEDs, Power, Systems, and Test and Measurement—and in late August asked our online readers to vote for their favorites. You responded in force. The pages that follow include our Readers' Choice in each category, as well as a collection of other popular Design Ideas.

As always, you can find many more Design Ideas online at www.edn.com/designideas. You might even want to share a Design Idea of your own with the *EDN* community. For information on that process, take a look at page 26 of this supplement, or go to www.edn.com/4394666.

Steve Taranovich,
Senior Technical Editor, **EDN**

How to recover a pulse signal with a large capacitance load

Chenan Tong, Texas Instruments

In some applications, it is necessary to transmit square waves across a long cable. Long cables, however, typically have high capacitance, which can significantly affect the signal's wave shape. As such, the signal's frequency and duty cycle need to be maintained if the signal is to remain free from distortion. This Design Idea discusses this phenomenon and offers a simple solution.

Figure 1 illustrates a common solution used to reconstruct a square wave at the end of a long cable (47-pF cable capacitance). V_{IN0} is the signal to be transmitted. The signal at V_{IN1} represents the signal at the end of the cable. You can see that this signal is distorted by the charge and discharge of the parasitic capacitance of the cable. Furthermore, the gate (IC_2) sees the rising and falling edges differently, so the reconstructed output signal will not be an accurate representation of the original digital signal.

The results in **Figure 2** show that you cannot recover input pulse with a simple logic gate. You need to find a different method to detect the rising and falling edges of the digital circuits. A differentiator can be used to detect the square-wave edges because the output of the RC circuit rises after the rising edge and falls after the falling edge of the square wave. Remember that the differentiator output is proportionate to the rate of change of the output signal, so it moves positively for increasing signals and negatively for decreasing signals.

The design in **Figure 3** uses a differentiator. **Figure 3** also shows the simple gate solution (IC_2) for comparison. In this example circuit, you can see how the simple gate solution does not effectively solve the problem. Note that the signal at V_{IN1} is from the charging and discharging of C_2 times R_6. In this

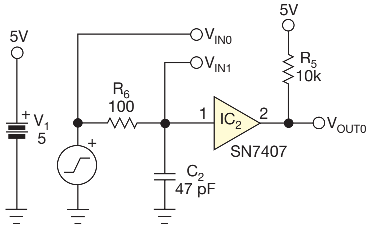

Figure 1 Shown is a common pulse-reconstruction solution.

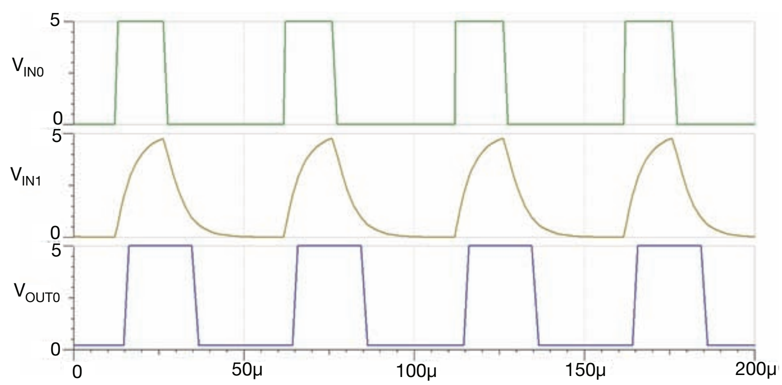

Figure 2 Simulation results for the common pulse reconstruction show that you cannot recover the input pulse with a simple logic gate.

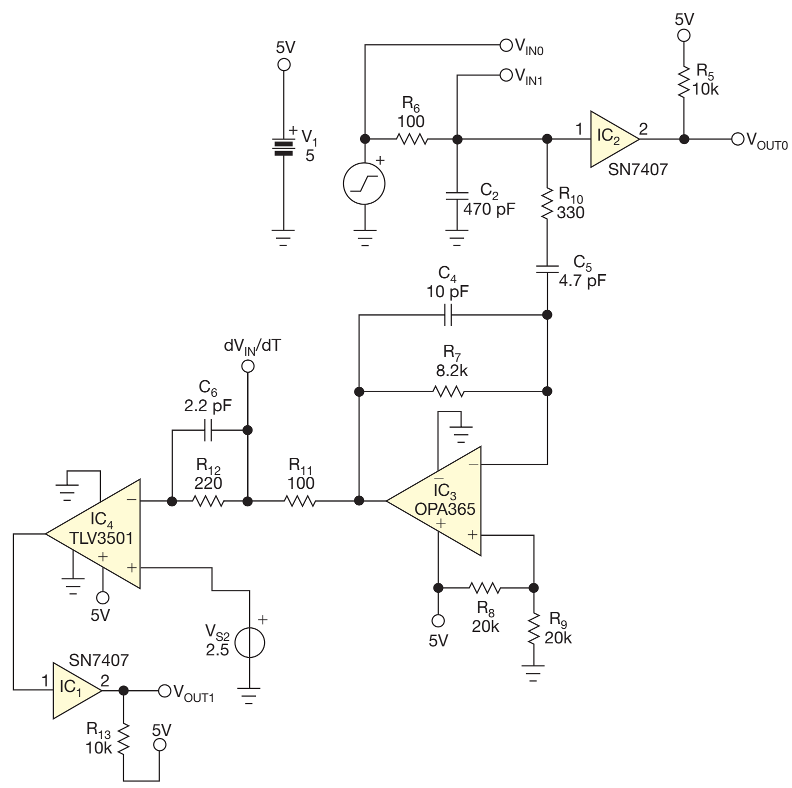

Figure 3 By differentiating the RC signal, you can reconstruct a signal that more closely resembles the original square wave.

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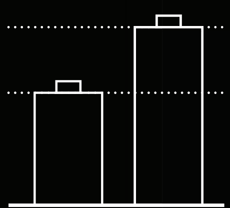

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example, C_2 is 470 pF, or 10 times larger than the example in **Figure 1**. When the input pulse is high (after the rising edge), the capacitor voltage increases. The differentiator output is negative for increasing capacitor voltage. When the input pulse is low (after the falling edge), the capacitor voltage decreases. The differentiator output is positive for increasing capacitor voltage.

Thus, by differentiating the RC signal you can reconstruct a signal that more closely resembles the original square wave. A comparator follows the differentiator output to create a sharp square-wave output.

Figure 4 shows the simulation results for the circuit in **Figure 3**. The input signal is a 20-kHz square wave with a duty cycle of 20%. The output of IC_2 clearly does not reproduce the original signal. In fact, IC_2 does not even detect most of the pulses. The differentiator's output looks like a smoothed inversion of the original digital signal. The comparator converts the differentiator output to a sharp square wave that accurately matches the frequency and duty cycle of the original signal. Specifically, the overall error in the duty cycle for this example is approximately 10%.

With this circuit, you can easily implement pulse recognition after a long cable and heavy capacitance load. This method produces pulse transmission with low distortion so that the frequency and duty cycle of the original signal are preserved. EDN

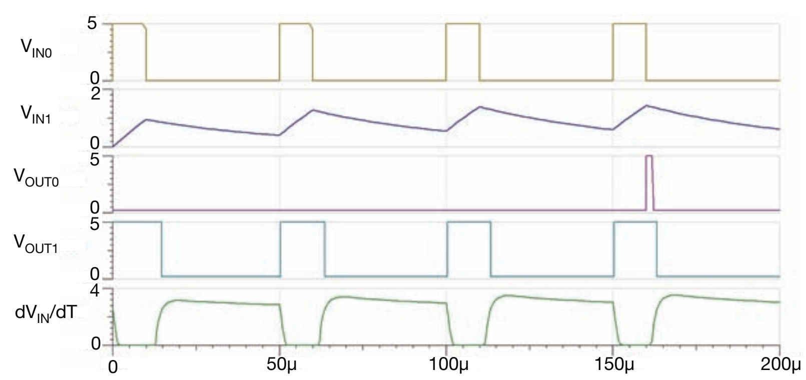

Figure 4 In these simulation results for differentiator-plus-comparator reconstruction, the differentiator output looks like a smoothed inversion of the original digital signal.

ACKNOWLEDGMENT

Special thanks to Arthur Kay and Matthew Hann of Texas Instruments for contributing their technical expertise in this subject area.

REFERENCES

1 "Tutorial 7 of 8: The Op-amp Differentiator Amplifier," Electronics-Tutorials.ws, http://bit.ly/PT8kLM.
2 OPA365 data sheet, Texas Instruments, http://bit.ly/UNNAWp.

Simple reverse-polarity-protection circuit has no voltage drop

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

Common methods of reverse-voltage protection employ diodes to prevent damage to a circuit. In one approach, a series diode allows current to flow only if the correct polarity is applied (**Figure 1**). You can also use a diode bridge to rectify the input so that your circuit always receives the correct polarity (**Figure 2**). The drawback of these approaches is that they waste power in the voltage drop across the diodes. With an input current of 1A, the circuit in **Figure 1** wastes 0.7W, and the circuit in **Figure 2** wastes 1.4W.

This Design Idea suggests a simple method that has no voltage drop or wasted power (**Figure 3**).

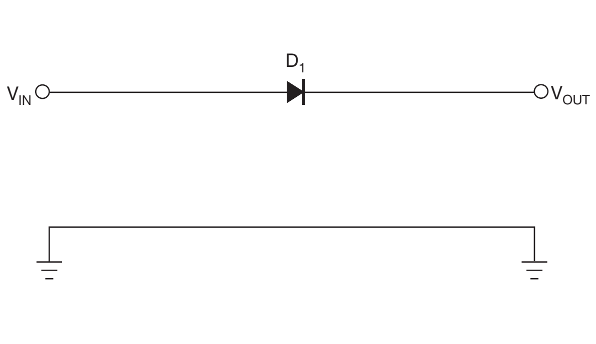

Figure 1 A series diode protects systems from reverse polarity but wastes power in diode losses.

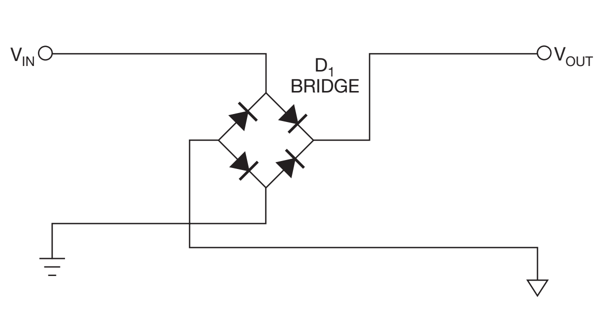

Figure 2 You can use a bridge rectifier so that your system works no matter what the input polarity is. This circuit wastes twice the power, in diode losses, of the circuit in Figure 1.

Select a relay to operate with the reverse-polarity voltage. For example, use a 12V relay for a 12V supply system. When you apply correct polarity to the circuit, D_1 becomes reverse-biased, and the S_1 relay remains off. Then connect the input- and output-power lines to the normally connected pins of the relay, so current flows to the end circuit. Diode D_1 blocks power to the relay, and the protection circuit dissipates no power.

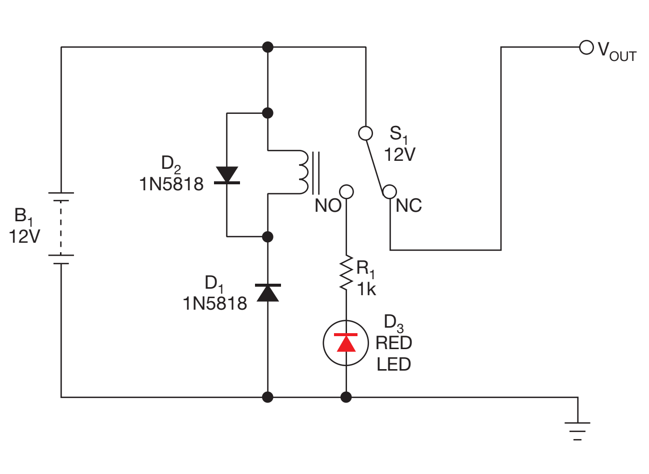

Figure 3 You can wire a relay switch to pass power to your system with no power loss. D_2 clamps inductive kicks from the relay coil.

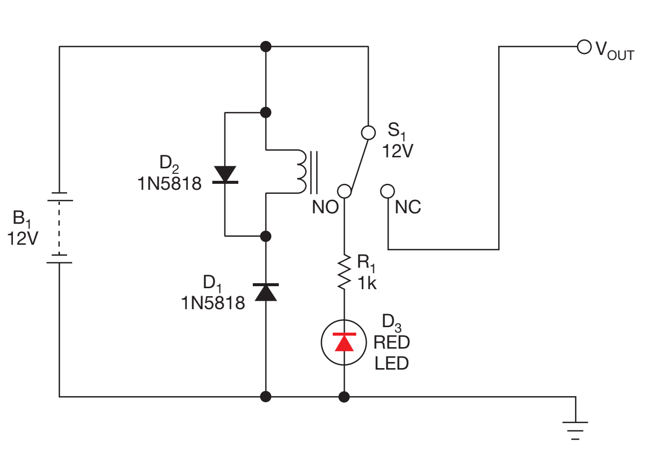

Figure 4 With reversed input voltage, the relay switch engages, interrupting power to the system, and the LED lights.

When you apply incorrect reversed polarity, diode D_1 becomes forward-biased, turning on the relay (**Figure 4**). Turning on the relay cuts the power supply to the end circuit, and red LED D_3 turns on, indicating a reverse voltage. The circuit consumes power only if reverse polarity is applied. Unlike FETs or semiconductor switches, relay contact switches have low on-resistance, meaning that they cause no voltage drop between the input supply and the circuit requiring protection. Thus, the design is suitable for systems with tight voltage margins. **EDN**

Obtain a gain of 450 from one vacuum tube

Lyle Russell Williams, St Charles, MO

A direct-conversion radio receiver required an audio gain of 450 from a pentode vacuum tube. A pentode has a high transconductance—that is, the ratio of the change in plate current to the change of the control grid voltage that caused it. To get high gain, however, it needs a high load impedance. RF applications with pentodes often used LC-tuned circuits in their plate loads in which the impedance at resonance and, therefore, the gain is high. It is typically impossible to implement a high load impedance using an untuned circuit because of the dc requirements of the tube.

RF APPLICATIONS WITH PENTODES OFTEN USED LC-TUNED CIRCUITS IN THEIR PLATE LOADS.

For instance, a 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA (**Figure 1**). If the quiescent dc plate voltage is to be 60V, the load resistance must be no more than 12 kΩ. The 0.5-MΩ plate resistance of the tube and the 1-MΩ load of the next stage are negligible with respect to the 12-kΩ load. With a transconductance of 3900 microsiemens, those requirements demand an audio gain of 45. You can easily achieve this gain with a triode tube.

To get a high load impedance with an untuned plate circuit, you can use a transistor current source for the tube (**Figure 2**). The transistor has no gain but functions as an active load for the tube and supplies the 5-mA plate current. You adjust the 500Ω potentiometer to obtain 60V dc at the plate. The gain of the circuit is approximately 450. This gain implies a 150-kΩ load impedance that the transistor supplies in parallel with the plate resistance and the resistance of the next stage. Alternatively, you can use two triode tube circuits in series, each having a gain of 21. **EDN**

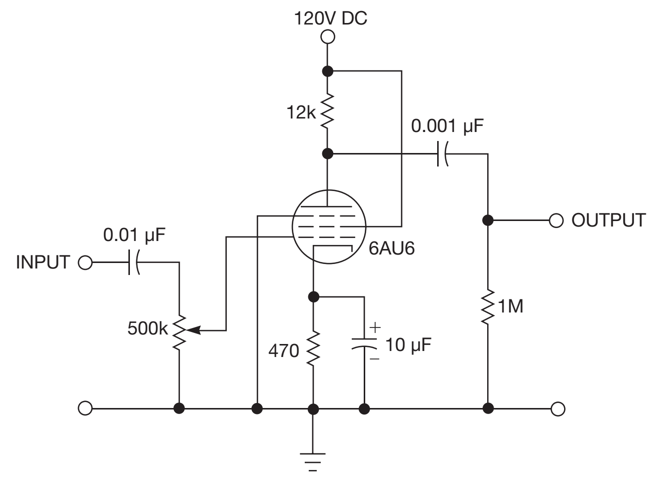

Figure 1 A 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA.

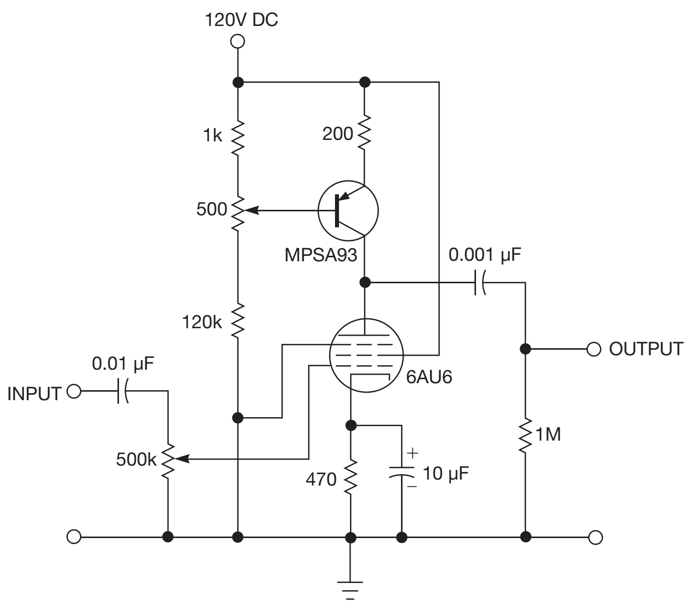

Figure 2 To get a high load impedance with an untuned plate circuit, you can use a transistor current source for the tube.

Build an op amp with three discrete transistors

Lyle Russell Williams, St Charles, MO

You can use three discrete transistors to build an operational amplifier with an open-loop gain greater than 1 million (**Figure 1**). You bias the output at approximately one-half the supply voltage using the combined voltage drops across zener diode D_1, the emitter-base voltage of input transistor Q_1, and the 1V drop across 1-MΩ feedback resistor R_2.

Resistor R_3 and capacitor C_1 form a compensation network that prevents the circuit from oscillating. The values in the **figure** still provide a good square-wave response. The ratio of R_2 to R_1 determines the inverting gain, which is –10 in this example.

You can configure this op amp as an active filter or as an oscillator. It drives a load of 1 kΩ. The square-wave response is good at 10 kHz, and the output reduces by 3 dB at 50 kHz. Set the 50-Hz low-frequency response with the values of the input and the output capacitors. You can raise the high-frequency response by using faster transistors and doing careful layout. **EDN**

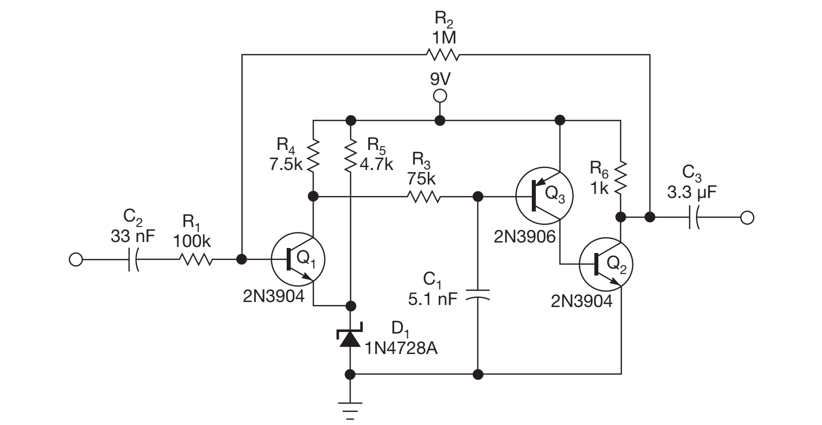

Figure 1 This ac-coupled inverting op amp has an open-loop gain of 1 million. R_1 and R_2 set a closed-loop gain of –10.

Automatic night-light feeds directly from the ac line

Abel Raynus, Armatron International Inc, Malden, MA

There are many approaches to the problem of activating a light when it becomes dark, and a recent Design Idea covers this topic (**Reference 1**). Some approaches require a dc power supply and an electromechanical relay, but a better approach involves feeding the device directly from the ac line, minimizing the number of components (**Figure 1**).

The heart of the device is a light-sensitive cadmium-sulphide resistor, P_R, with a resistance of approximately 200 kΩ in the dark, decreasing to a few kilohms in the light. P_R and capacitor C_1 form an ac-voltage divider. In daylight, the voltage across P_R is too low to generate the required gate-trigger current to turn on bidirectional ac switch Q_1, thus keeping the load—usually a lamp—off. When it becomes dark, P_R's resistance rises, resulting in an increase in the TRIAC's gate current that triggers the TRIAC and lights the lamp.

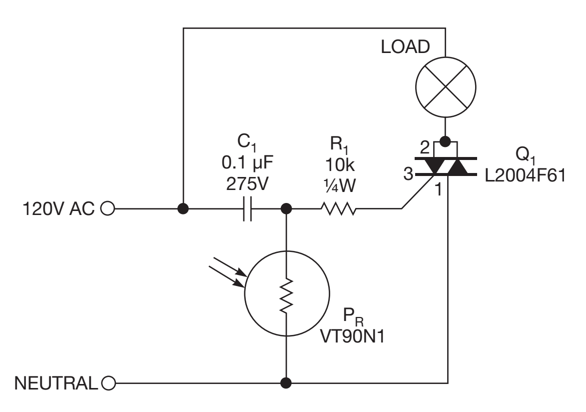

Figure 1 The photoresistor activates the TRIAC and the load when darkness falls.

The circuit uses inexpensive, off-the-shelf components, including the VT90N1 photoresistor; a 0.1-µF, 275V capacitor; and an L2004F61 TRIAC with a load current of 4A rms, a peak blocking voltage of 200V, and a gate-trigger current of 5 mA. The exact specifications of these components are not critical; you could use others instead.

Editor's note: Attributes worth mentioning include the fact that the capacitor introduces a phase shift, which places the peak of the gate voltage close to the zero crossing of the load's sine wave for optimum turn-on timing. Another benefit is thermal hysteresis, which occurs due to the reduction of the required triggering voltage and current as the TRIAC warms up after the initial turn-on. **EDN**

REFERENCE

1 Tran, Chau, "Simple night-light uses a photoresistor to detect dusk," *EDN*, Dec 15, 2011, pg 49, http://bit.ly/HPi1GG.

Use a transistor as a heater

REC Johnson, B Lora Narayana, and Devender Sundi,
Center for Cellular and Molecular Biology, Hyderabad, India

It is common to use transistors for driving resistive heating elements. However, you can use the heat that a power transistor dissipates to advantage in several situations, eliminating the need for a separate heating element because most transistors can safely operate at temperatures as high as 100°C.

A typical example is in a biological laboratory, in which maintaining the temperature of samples in microliter-sized cuvettes is a common requirement. The space/geometry constraint and the <100°C upper-temperature limit are the basic factors of the idea.

You can use an N-channel IRF540 MOSFET to directly heat and control the temperature of a biological sample from ambient to 45°C. **Figure 1** shows a simple on/off-type control circuit in which an LM35, IC_1, is the temperature sensor, whose output a DPM (digital panel meter) can display. IC_2 compares the voltage that VR_1 sets with the output of the LM35 to turn on Q_2 accordingly, with the positive feedback through R_9 providing a small amount of hysteresis. S_1 switches the DPM between a set value and the actual temperature readout. You derive the reference voltage from a TL431 shunt regulator (not shown). The LED lights up when Q_2 is on.

IC_1 and Q_2 thermally mount on the metal block that forms the sample holder; use thermal grease on both components for maximum heat transfer. Note that the mounting tab of the TO-220 package electrically connects to the drain, and you may need to insulate it from the cuvette with a thermal pad. Setting bias control VR_3 for a Q_2 current of 270 mA is sufficient to hold the cuvette at 45°C.

Be sure to set VR_3 to minimum power during initial power-up; if you set it for maximum power, you could apply 24V to Q_2's gate-to-source voltage, which is rated for a maximum of only 20V. You can extend the temperature range by changing the voltage divider comprising R_1, R_2, and VR_1. The design includes a safety cutoff circuit (not shown) in case the temperature gets too high.

YOU CAN USE THE HEAT THAT A POWER TRANSISTOR DISSIPATES TO ELIMINATE THE NEED FOR A SEPARATE HEATING ELEMENT.

Various other options are also possible applications for this circuit. These applications include linear control, pulse-width modulation, and the use of a PID (proportional-integral-derivative) controller, to name a few. EDN

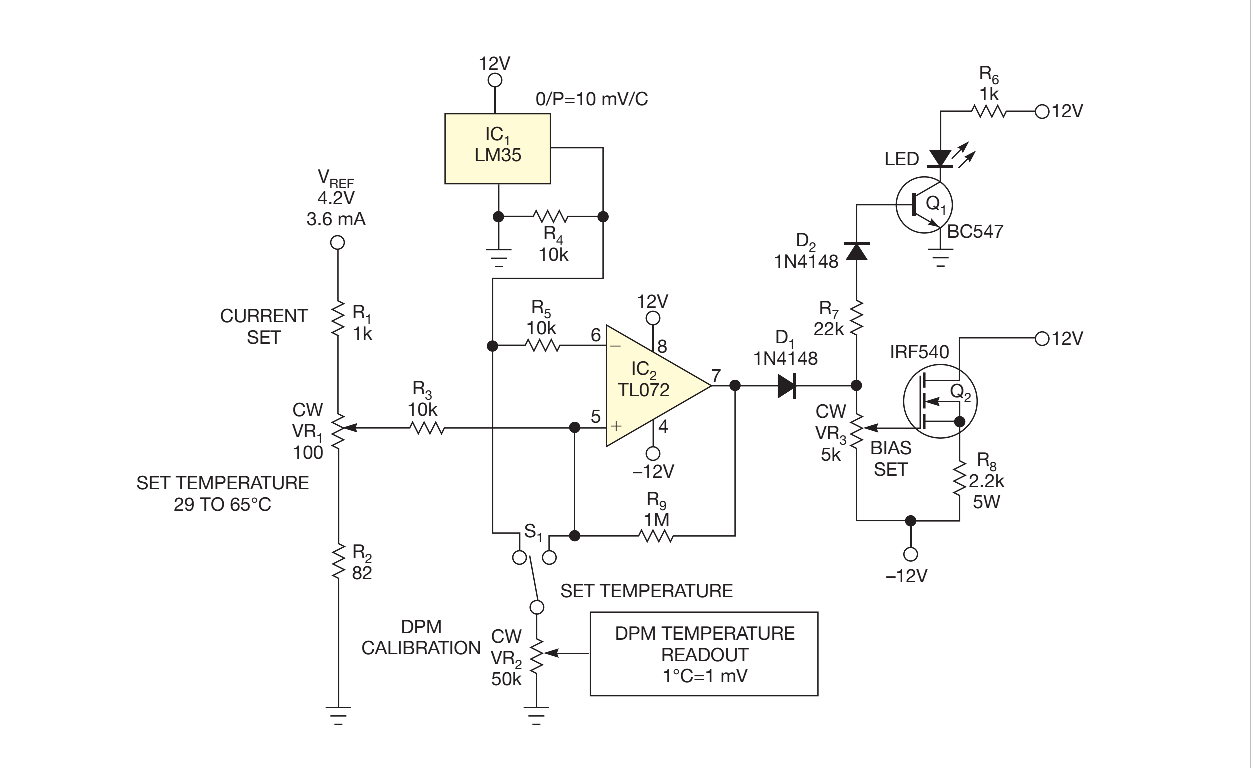

Figure 1 IC_1 senses the temperature of the item that Q_2 heats, and the temperature remains at the level that VR_1 sets.

READERS' CHOICE

Adjust power-efficient LED switch to any light intensity

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

You can use an LED as a photoelectric sensor. A previous Design Idea shows that such a switch is highly power-efficient, consuming almost no power (**Reference 1**). You cannot, however, adjust that configuration to switch at the desired light intensity. You can adjust the circuit in this Design Idea to any threshold level of light intensity necessary to maintain the on state of the photoelectric switch while retaining almost the same power efficiency of the original circuit (**Figure 1**).

Illuminating the reverse-biased green LED with ambient light causes the small current that flows through the LED to form the base current of the BC549 NPN transistor, which is amplified and passed on to the base of the BC177 PNP transistor. A magnified version of this current flows through the emitter of the BC177. The voltage drop across the emitter resistor depends on its value and the current flowing through it, which in turn determines the voltage drop across the CE terminals of the BC549.

By adjusting the value of the series emitter resistor, you can set a voltage corresponding to logic zero of a CMOS gate for any desired intensity of light falling on the green LED. This intensity depends heavily on the response of the green LED and the current gains of the two transistors, so you select the resistor value by shorting out combinations of the series string of resistors and use the 10-MΩ potentiometer as a fine adjustment. Once you find a suitable value, you can remove the unused resistors from your circuit.

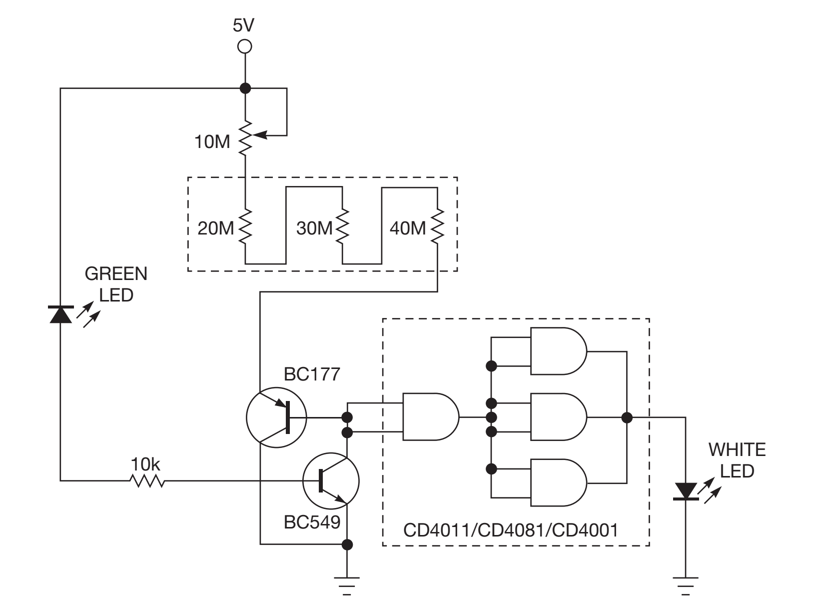

Figure 1 The photocurrent through the green LED amplifies to CMOS-logic levels to turn on the white LED when ambient light falls.

When the ambient-light intensity falls below this level, both the base current of the BC549 and the current through the emitter series resistors decrease. This decrease raises the input voltage at the CD4011 logic gate higher than the CMOS switching threshold. The typical gate sourcing current at a 3V output is approximately 3 to 4 mA per gate; running three gates in parallel delivers approximately 10 mA to the white LED. You can use inverting or noninverting gates for the same result. The circuit still retains its power efficiency because the required series-resistor values normally exceed 10 MΩ.

You can check a green LED's suitability for use as a photodiode by measuring the voltage drop across the LED with a 200-mV digital multimeter. If the LED is suitable as a photoelectric sensor, you will see a voltage of 0.3 to 1 mV across it, and this voltage changes with the intensity of light falling on the LED. EDN

REFERENCE

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Drive 16 LEDs with one I/O line

Zoran Mijanovic and Nedjeljko Lekic,
University of Montenegro, Podgorica, Montenegro

Over the last few years, several Design Ideas have described how to use just a few microcontroller I/O pins to drive many LEDs (**references 1 through 7**). The circuit in **Figure 1** can drive 16 LEDs with just one pin and two shift registers. You can use the circuit to drive long-dot-bar or two seven-segment-digit displays. Adding multiplexing to the same circuit enables it to drive eight seven-segment LED digits.

The microcontroller drives the shift registers' clock inputs. That signal also passes through an RC filter and drives data inputs A and B. A 100-kΩ resistor, R, and the A and B input pins' capacitances form the RC filter (**Figure 2**), producing time delay of approximately R×C×ln2=100 kΩ×(5 pF+5 pF)×0.7=0.7 μsec.

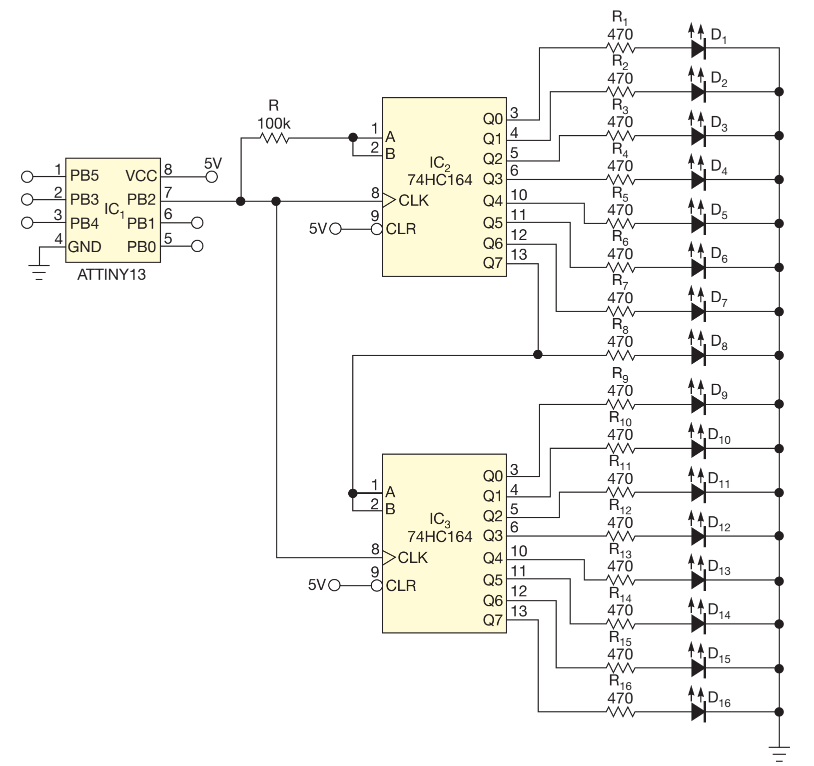

Figure 1 A 16-LED dot-bar/bar-graph display uses two 8-bit serial-input/parallel-output shift registers.

To write a logic zero to the shift register, the microcontroller holds a low level for approximately 2 µsec, which is longer than the time delay. It then sets the signal to a logic one, or high, level. To write a logic one, the microcontroller holds the high level for longer than the time delay. The MCU then makes negative pulses of approximately 0.25 µsec, or two CPU cycles, which is shorter than the time delay and which doesn't change the logic level at the data inputs.

Figure 3 shows the clock signal in Channel 1 (yellow) and the data signal in Channel 2 (blue). The oscilloscope is a Tektronix (www.tektronix.com) DPO4034 with TPP0850 high-voltage probes. These probes have 40-MΩ input resistance and only 1.5-pF input capacitance, minimizing distortion.

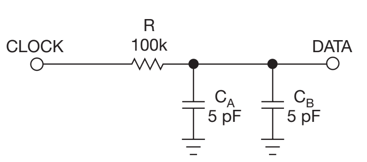

Figure 2 An RC filter provides a 0.7-µsec delay.

A rising edge on the clock signal clocks the shift registers. This edge corresponds to the data signal's local minimum. **Figure 3** also shows that the minimum data-signal voltages for logic zero and logic one are 1.3 and 3.1V, respectively. The shift register's logical threshold is 2.5V.

These voltages guarantee sufficient voltage margins. If your design requires higher margins, vary the signal timing and use a higher resistance for R in **Figure 1**. This circuit stores 16 bits in shift registers in approximately 35 µsec.

You can view a short video of the circuit in operation and download a code listing, in C, at the online version of this Design Idea at www.edn.com/4368093. The software turns on the LEDs one by one every 500 msec until all LEDs are on. It then turns off all the LEDs and repeats the cycle. **EDN**

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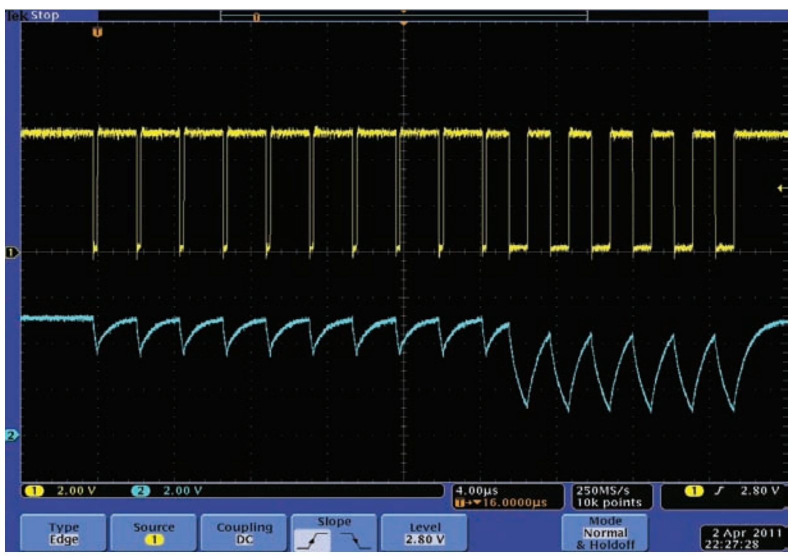

Figure 3 The waveform shows the circuit writing the pattern 1111111111000000 for the display. The upper, yellow trace is the clock signal, and the lower, blue trace is the data signal.

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Offline supply drives LEDs

TA Babu, Chennai, India

LEDs need power when rectified ac-mains voltage drops during its cycle. The circuit in **Figure 1** lets you use an inductorless, switching, offline power supply as an LED driver for emergency-exit signs and neon-light replacements. The design uses off-the-shelf components, offers efficient operation without an inductor in the dc side of the circuit, has no high-voltage capacitors, operates directly from either 120 or 230V ac, has minimal power dissipation, and has adjustable output voltage.

The circuit operates by controlling the conduction angle of MOSFET Q_2. When the rectified ac voltage is below the high-voltage threshold, V_{TH}, which D_1 sets, the series pass transistor turns on. The series pass transistor turns off when the output storage capacitor, C_2, charges up to the regulation point.

THE DESIGN DOES NOT REQUIRE AN INDUCTOR IN THE DC SIDE OF THE CIRCUIT.

The circuit’s output voltage decays when Q_2 is off and when the rectified ac is below the output voltage (**Figure 2**). The load and the value of C_2 determine the amount of decay. The switch conducts only when it has low voltages across it, minimizing power dissipation. The output capacitor charges on the rising edge of a sine wave, which achieves reasonable efficiencies. Fusible resistor R_1 provides catastrophic-failure protection and limits input inrush when you first apply ac power. A 15V diode, D_2, limits the voltage to the gate of Q_2 and limits the voltage across transistor Q_1.

The current interruption in the MOSFET causes ringing on the drain-to-source voltage of Q_2, creating conducted EMI (electromagnetic interference). The 2.2-mH choke, L_1, and capacitor C_1 suppress EMI. This design maintains a fairly constant illumination over a wide voltage variation in the input. If necessary, you can add a few more such strings to suit your requirements.

Note that this circuit does not provide galvanic isolation. Touching any part of the circuit during operation can give you an electric shock. EDN

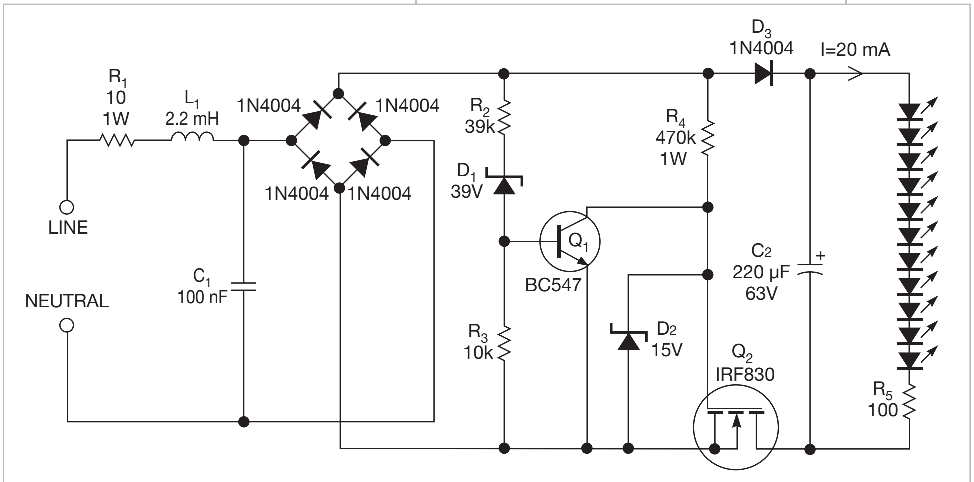

Figure 1 The transistor and MOSFET provide current to keep the LEDs lit.

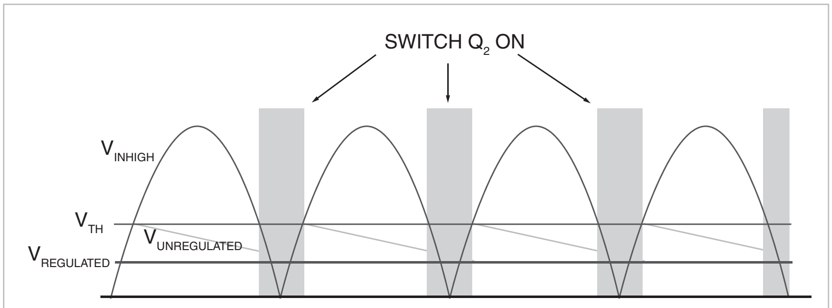

Figure 2 Switch Q_2 turns on when the rectified ac input voltage drops below a threshold.

READERS' CHOICE

Convert 1 to 5V signal to 4- to 20-mA output

Thomas Mosteller, Linear Technology Corp

Despite the long-predicted demise of the 4- to 20-mA current loop, this analog interface is still the most common method of connecting current-loop sources to a sensing circuit. This interface requires the conversion of a voltage signal—typically, 1 to 5V—to a 4- to 20-mA output. Stringent accuracy requirements dictate the use of either expensive precision resistors or a trimming potentiometer to calibrate out the initial error of less precise devices to meet the design goals.

Neither technique is optimal in today's surface-mounted, automatic-test-equipment-driven production environment. It's difficult to get precise resistors in surface-mount packages, and trimming potentiometers require human intervention, a requirement that is incompatible with production goals.

The Linear Technology LT5400 quad matched resistor network helps to solve these issues in a simple circuit that requires no trim adjustments but achieves a total error of less than 0.2% (**Figure 1**). The circuit uses two amplifier stages to exploit the unique matching characteristics of the LT5400. The first stage applies a 1 to 5V output—typically, from a DAC—to the noninverting input of op amp IC_{1A}. This voltage sets the current through R_1 to exactly V_{IN}/R_1 through FET Q_2. The same current is pulled down through R_2, so the voltage at the bottom of R_2 is the 24V loop supply minus the input voltage.

This portion of the circuit has three main error sources: the matching of R_1 and R_2, IC_{1A}'s offset voltage, and Q_2's leakage. The exact values of R_1 and R_2 are not critical, but they must exactly match each other. The LT5400A grade achieves this goal with ±0.01% error. The LT1490A has <700-μV offset voltage over 0°C to 70°C. This voltage contributes 0.07% error at an input voltage of 1V. The NDS7002A has a leakage current of 10 nA, although it is usually much less. This leakage current represents an error of 0.001%.

The second stage holds the voltage on R_3 equal to the voltage on R_2 by pulling current through Q_1. Because the voltage across R_2 equals the input voltage, the current through Q_1 is exactly the input voltage divided by R_3. By using a precision 250Ω current shunt for R_3, the current accurately tracks the input voltage.

The error sources for the second stage are R_3's value, IC_{1B}'s offset voltage, and Q_1's leakage current. Resistor R_3 directly sets the output current, so its value is crucial to the precision of the circuit. This circuit takes advantage of the commonly used 250Ω current-loop-completion shunt resistor. The Riedon SF-2 part in the **figure** has 0.1% initial accuracy and low temperature drift. As in the first stage, offset voltage contributes no more than 0.07% error. Q_1 has less than 100-nA leakage, yielding a maximum error of 0.0025%.

Total output error is better than 0.2% without any trimming. Current-sensing resistor R_3 is the dominant source of error. If you use a higher-quality device, such as the Vishay PLT series, you can achieve an accuracy of 0.1%. Current-loop outputs are subject to considerable stresses in use. Diodes D_1 and D_2 from the output to the 24V loop supply and ground help protect Q_1; R_6 provides some isolation. You can achieve more isolation by increasing the value of R_6, with the trade-off of some compliance voltage at the output. If the maximum output-voltage requirement is less than 10V, you can increase R_6's value to 100Ω, affording

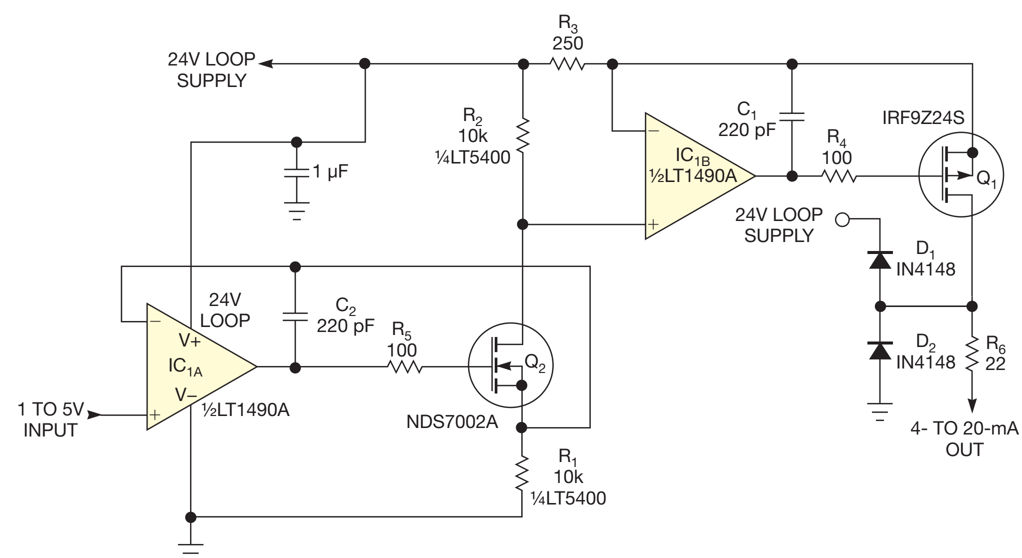

Figure 1 Precision matched resistors provide accurate voltage-to-current conversion.

even more isolation from output stress. If your design requires increased protection, you can fit a transient-voltage suppressor to the output with some loss of accuracy due to leakage current.

This design uses only two of the four matched resistors in the LT5400 package. You can use the other two for other circuit functions, such as a precision inverter, or another 4- to 20-mA converter. Alternatively, you can place the other resistors in parallel with R_1 and R_2. This approach lowers the resistor's statistical-error contribution by the square root of two. EDN

Inverting level-shift circuit has negative potential

Chun-Fu Lin and Shir-Kuan Lin, National Chiao Tung University, Hsinchu, Taiwan; and Hui-Shun Huang, Jyi-Jinn Chang, and Tai-Shan Liao, National Applied Research Laboratories, Hsinchu

Digital-system designs require you to consider many core voltages. Memory operates at 1.8V, I^2C and FPGA devices operate at 3.3V, microcontrollers operate at 5V, and charge-coupled-device image sensors operate at –9 to 8V. Clocks for each device must suit their operating voltages.

You can use the level-shift circuit in **Figure 1** to adjust an input clock signal to the proper logic-high and logic-low voltage levels, including negative voltages. This property is handy for devices that need a negative voltage, such as a charge-coupled-device sensor. Although the circuit's output clock is 180°-inverted relative to the input clock, that inversion does not affect the function of the device.

The level-shift circuit comprises fast-switching transistors Q_1 and Q_2. The user chooses level-shift high and level-shift low, which are dc-bias voltages and which connect to the transistor emitters, to match the desired output high- and low-logic levels. C_1, R_1, D_1, C_2, R_2, and D_2 keep the base voltages of Q_1 and Q_2 close to that of their emitters.

Because memory and charge-coupled-device sensors usually have high-frequency clocks, you can choose C_1 and C_2 to prevent low-frequency-noise pass-through. The circuit in **Figure 1** uses a 20-MHz signal for measurements (**Table 1**) and thus uses a value of 100 pF for C_1 and C_2. When the input voltage's clock is low, Q_1 turns on and Q_2 turns off, driving the output voltage's clock to the level shift's high potential. When the input voltage's clock is high, Q_1 turns off and Q_2 turns on, driving the output voltage's clock to the level shift's low potential, even when that potential is negative relative to ground.

Because of the circuit's high switching speeds, keep component leads as short as possible to minimize inductance. This caveat is especially true for C_3 through C_6's leads to their respective transistor emitters and to the ground plane or the output ground return. EDN

TABLE 1 INPUT AND OUTPUT CLOCKS

High/low level shift (V)	Input clock (V)	Output clock (V)
3.3/0	0/5	3.3/0
20/10	0/5	20/10
–5/–10	0/5	–5/–10
2/–4	0/5	2/–4

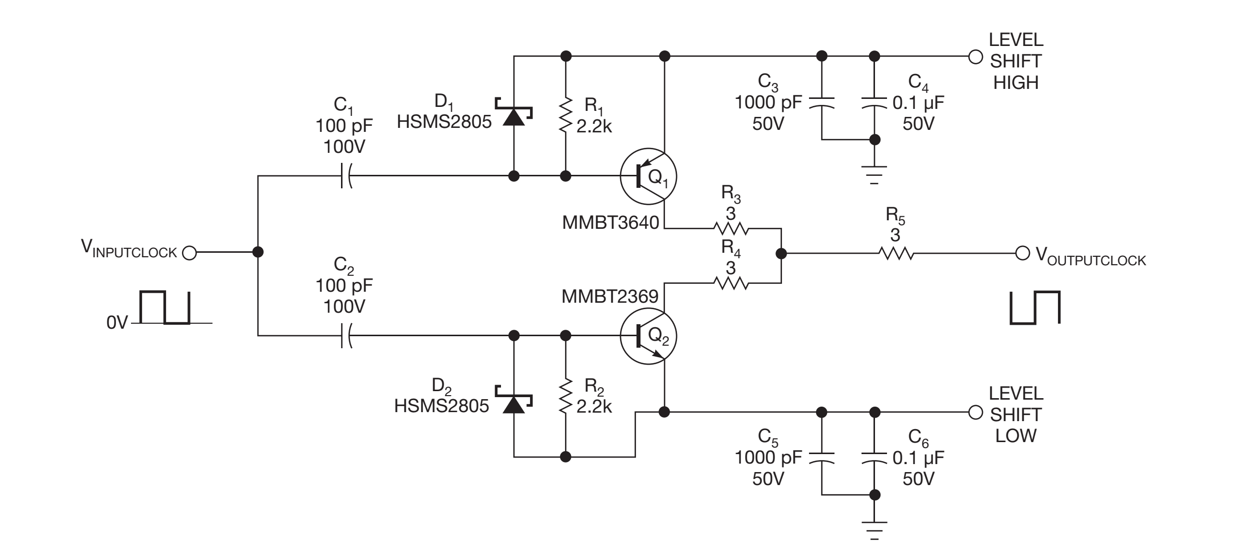

Figure 1 This simple and fast level-shift circuit can adjust an input clock to both positive and negative voltage levels.

Complementary-pair dc/dc converter simultaneously doubles, inverts supply voltage

Ajoy Raman, Bangalore, India

The circuit in this Design Idea uses an intrinsic property of collector voltages in one-transformer push-pull dc/dc converters: They have a swing of twice the supply voltage. When you implement these circuits with an NPN device, the collector swings from 0V to twice the supply-rail voltage. When you use PNP devices, the collector voltage swings from V_{CC} to an equal amplitude but negative V_{CC} (**Reference 1**). In this circuit, a complementary pair of transistors, simultaneously implementing a voltage doubler and a negative-voltage source, drives the two windings of the transformer.

One of the windings of transformer T_1 connects to ground, driven by PNP transistor Q_1 from V_{CC} (**Figure 1**). The other winding of T_1 connects to V_{CC}, and NPN transistor Q_3 drives the lower end to ground. Q_2 and Q_4 drive Q_1 and Q_3, respectively. The collectors of Q_3 and Q_1 through resistors R_4 and R_3 provide cross-coupled drives to Q_2 and Q_4. R_1 and R_2 form the collector loads for Q_2 and Q_4. D_1 and D_4 prevent the reverse breakdown of Q_1 and Q_3. The drive configuration and the transformer's winding polarity provide regenerative feedback and self-oscillation so that the transformer alternates between positive and negative saturation, inducing voltages to drive transistors Q_1 and Q_3 alternately on and off.

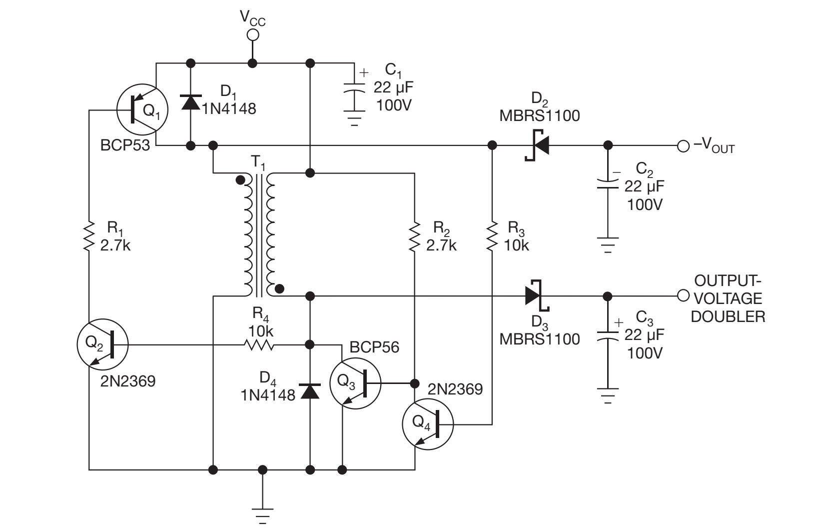

Figure 1 Cross-coupled regeneration drives switching transistors Q_1 and Q_3 and the windings of the transformer. The resulting voltage swings at their collectors are rectified to twice the positive and the negative power-supply rails.

A square wave with an amplitude twice V_{CC} is generated at the collector of Q_1, which swings nominally from V_{CC} to the equal but negative output voltage. Simultaneously, a square wave with an amplitude twice the supply-rail voltage is generated at the collector of Q_3, which swings nominally from 0V to twice the supply-rail voltage.

D_2 and C_2 provide half-wave rectification and filtering of the Q_1 collector waveform generating the negative voltage output. Half-wave rectification and filtering of the Q_3 collector waveform using D_3 and C_3 generate the doubler's output.

T_1 is 200 turns of bifilar AWG 37 enameled wire wound 1-to-1 on a ferrite toroid core (**references 2** and **3**). **Table 1** shows the experimental results with the voltage doubler and negative-voltage-generation circuit operating over an input voltage of 5 to 30V, demonstrating operation over a wide input voltage range and providing power at both outputs simultaneously at moderate efficiency. EDN

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3 MN60 manganese-zinc material specs, Ceramic Magnetics Inc, http://bit.ly/KoyO4Y.

TABLE 1 EXPERIMENTAL RESULTS

Input voltage (V)	Input current (mA)	Frequency (kHz)	Voltage doubler (V)	Current doubler (mA)	Negative voltage (V)	Negative current (mA)	Input power (W)	Output power (W)	Efficiency (%)
5	253	2.1	7.68	81.7	–3.41	–72.5	1.27	0.87	69
9.97	360	4.05	17.33	115.5	–8.65	–86.5	3.59	2.75	76.6
15	420	6.02	27.2	136	–13.58	–90.5	6.3	4.93	78.2
19.4	400	7.37	34.9	145.4	–18.33	–61.1	7.76	6.19	79.8
25	340	10.47	48.5	97	–23.8	–79.3	8.5	6.59	77.5
30	410	12.07	56.5	113	–27.6	–92	12.3	8.92	72.5

READERS' CHOICE

Wireless temperature monitor has data-logging capabilities

Tom Au-Yeung and Wilson Tang, Maxim Integrated Products, Sunnyvale, CA

You can use a local temperature sensor and an ASK (amplitude-shift-keying) transmitter/receiver pair to design a simple wireless temperature-monitoring system with data-logging capabilities. A microcontroller processes and displays the temperature reading to the user. The microcontroller's onboard UART (universal asynchronous receiver/transmitter) also allows for data-logging applications.

Local-temperature sensor IC_1 detects the ambient temperature at the device (**Figure 1**). The output of IC_1 is a square wave with a frequency proportional to temperature in kelvins. ASK transmitter IC_2 modulates the signal onto the carrier frequency of 315 MHz. You measure the output signal's frequency with a frequency counter. The configured scalar multiplier is 1K/Hz when the TS1 pin connects to ground and the TS0 pin connects to V_{DD}. This scalar multiplier is configurable with pins TS1 and TS0. ASK receiver IC_3 demodulates the signal at the corresponding carrier frequency (**Figure 2**).

Comparator IC_4 connects to IC_3's RSSI

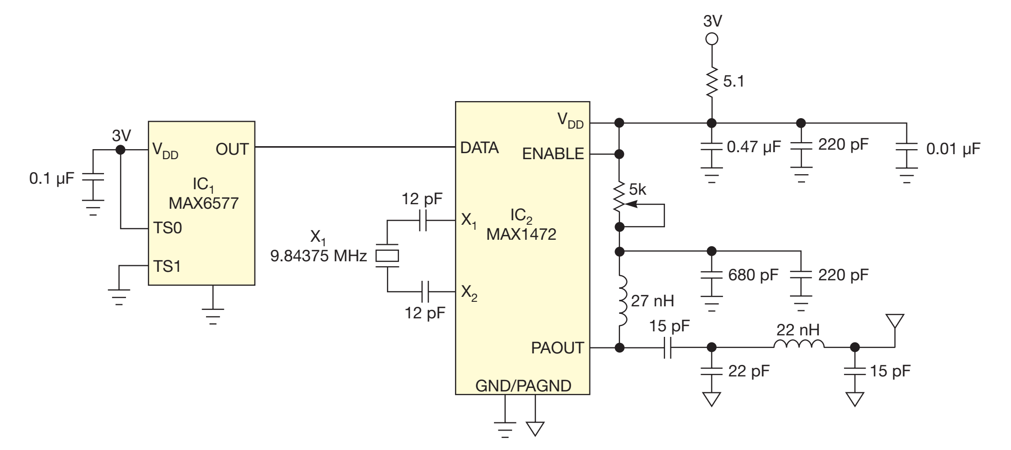

Figure 1 The MAX6577 temperature sensor and 315-MHz MAX1472 ASK transmitter form a wireless temperature-monitoring system.

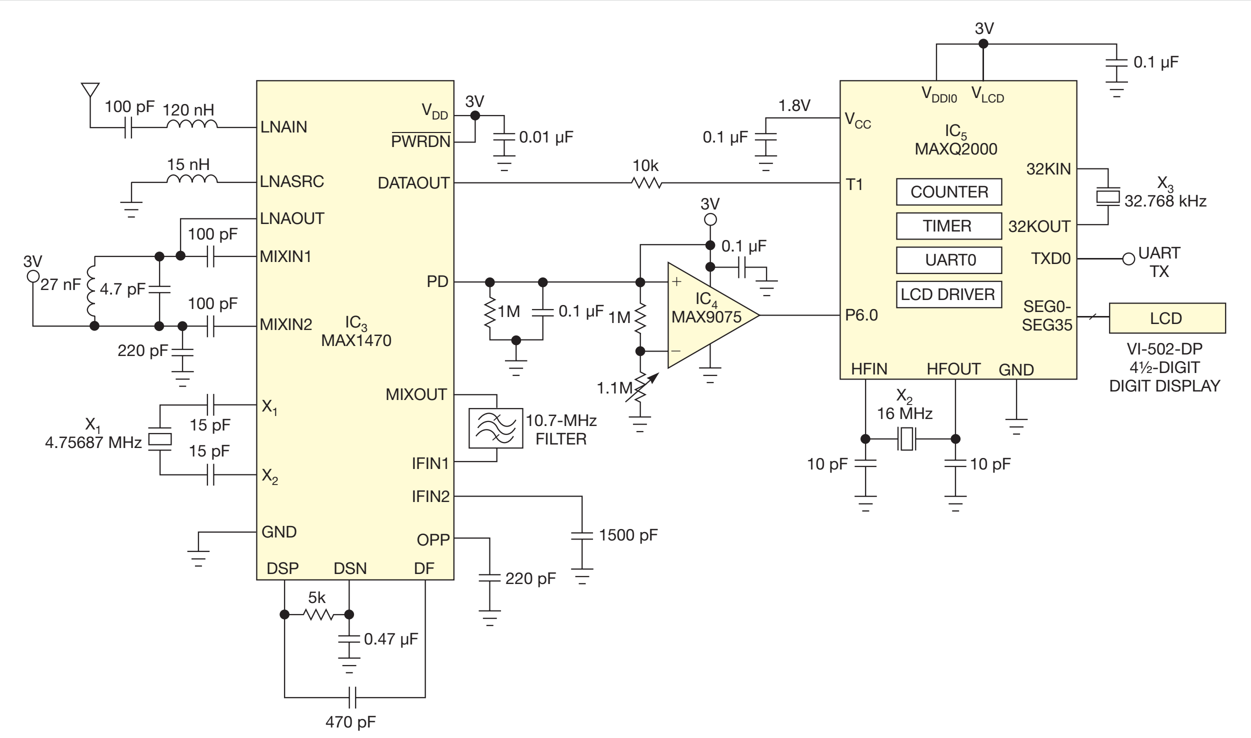

Figure 2 An ASK receiver with a microcontroller processes and displays temperature data.

(received-signal-strength indicator) with an internal peak detector. The external RC follows the peak power of the received signal and compares it with a predetermined, resistor-voltage-divider-generated voltage level. Lab experiments show that a threshold of approximately 1.57V generates a valid output on the data-out pin without receiving false readings. Adjust this threshold to the proper level for optimal performance. The comparator's output is low when the received signal is weak or invalid and high when the received signal is adequate.

Microcontroller IC_5 then measures and displays the value of the signal frequency using its integrated timer/counters and LCD-driver peripherals. A counter tracks the number of rising-edge transitions on the input temperature signal, and a timer tracks the elapsed time. After the timer's 1-sec period elapses, an interrupt occurs. At that moment, the circuit reads the counter value, converts it to Celsius, and displays it on the LCD. The counter then resets to zero to restart the process. The timer automatically reloads once the timer interrupt occurs. UART0 also outputs the resulting temperature. A handheld frequency counter verifies the temperature reading.

The microcontroller monitors the signal power through P6.0, a general-purpose input pin. When the input is logic low, the LCD and UART output "no RF" to alert users of possible transmitter issues when the transmitter and receiver are too far apart from each other. The LCD connection follows the design in the IC's evaluation kit. Using a look-up table in the data segment of the assembly code enables you to preserve the internal mapping of the display's A through G segments. This preservation ensures that the display enables the correct segments. Using an RS-232 level converter, the UART output sends data to a data-logging device, such as a computer.

Use the MAX-IDE assembler software to program the device during assembly. The MAXQJTAG board operates with the MAX-IDE to load the code onto the device. You can download the project files at www.edn.com/4368878. This design provides for a 1-sec temperature-refresh rate in 1°C increments, which is within the accuracy of IC_1.EDN

Microcontroller drives piezoelectric buzzer at high voltage through one pin

Mehmet Efe Ozbek, PhD, Atilim University, Ankara, Turkey

A previous Design Idea demonstrates how you can use a microcontroller to drive a piezoelectric buzzer at a high alternating voltage through a four-MOSFET circuit that interfaces to two of its I/O pins (**Reference 1**). This expanded Design Idea provides a modification of the previous circuit to save one of the I/O pins of the microcontroller. Q_4's gate connects to Q_2's drain rather than a second I/O pin (**Figure 1**). The microcontroller turns on Q_2 by applying a high logic level to the I/O pin, pulling Node A down to a low logic level. This action turns on Q_3 and turns off Q_4. The voltage on Node B becomes 15V, and Q_1 turns off. The voltage across the piezoelectric element is now 15V.

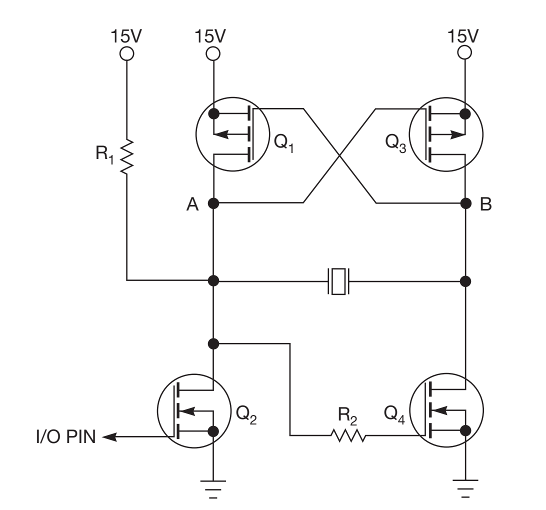

Figure 1 One microprocessor I/O pin drives this circuit to generate an alternating voltage across the piezoelectric buzzer.

The microcontroller then toggles the I/O pin low, turning off Q_2. Q_1 is also off, so Node A slowly rises to a high logic level through pullup resistor R_1. When the voltage on Node A reaches the switching threshold of the inverter comprising the Q_3 and Q_4 pair, Q_3 quickly turns off and Q_4 quickly turns on. The consequently low logic level on Node B turns on Q_1 and speeds the increase of Node A's voltage. The 15V across the piezoelectric buzzer is now of the opposite polarity.

R_2 weakens the coupling between the output and the input of Q_4 due to the presence of the piezoelectric element. A value of 330Ω for R_2 is usually sufficient to suppress high-frequency oscillations that the feedback causes. The drained power from the supply increases if you use low values for R_1. Using excessively large values for R_1 also increases power dissipation by prolonging the switching of the transistors and associated shoot-through currents. The optimum value for R_1 is approximately 1 kΩ.

Saving an I/O pin with this design involves the trade-off of increased power consumption. The circuit's power consumption is thus one order of magnitude greater than the circuit described in the previous Design Idea.EDN

REFERENCE

1 Ozbek, Mehmet Efe, "Microcontroller drives piezoelectric buzzer at high voltage," *EDN*, March 1, 2012, pg 44, http://bit.ly/JyzLpz.

Logic gates form high-impedance voltmeter

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

You can use the circuit described in this Design Idea to estimate voltages across 10- to 100-MΩ resistances. It also works for reverse-biased diodes.

ESTIMATE THE UNKNOWN VOLTAGE USING A GRAPH OF THRESHOLD VERSUS SUPPLY VOLTAGE.

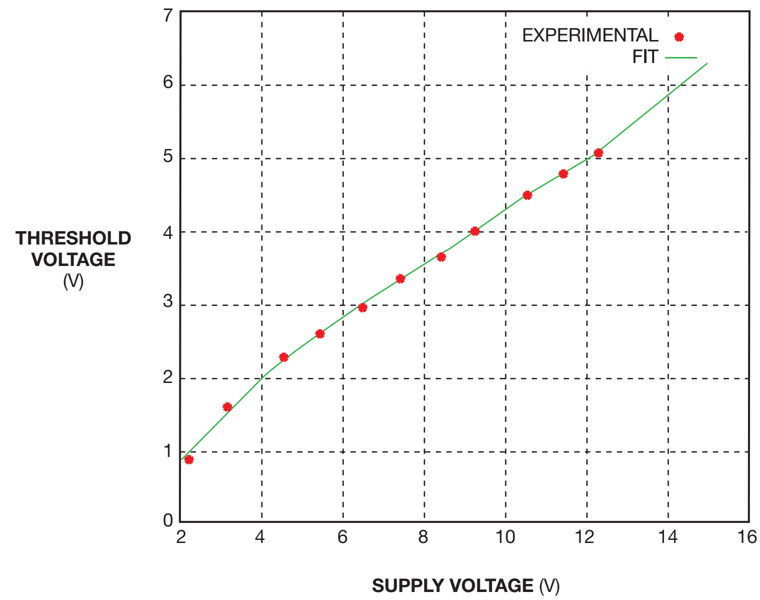

Figure 2 The gate's threshold voltage is nearly linear respective to the power-supply voltage. Download this plot from the online Design Idea at www.edn.com/4368072.

The common CMOS gates in **Figure 1** have an input threshold voltage in which the output swings from logic zero to logic one, and vice versa. The threshold voltage depends on the supply voltage (**Figure 2**). Because of each CMOS gate's high input impedance, input currents are approximately 0.01 nA. If you apply 5V to 100 MΩ, you get 50 nA. Thus, you can connect the gate input at a point at which it draws a negligible amount of current.

You can vary the CMOS gate's supply voltage to attain the desired threshold voltage for the gate input. If you apply the unknown voltage to one of the gate's inputs and then connect the other input to the positive-voltage supply, you can vary the supply voltage, V_S, until you reach a point at which the threshold voltage at the input becomes equal to the unknown voltage.

At this point, the output of the sense gate, IC_{1A}, changes from logic zero to logic one. When this event happens, the threshold of the gate passes the unknown voltage. You can estimate the unknown voltage using a graph of threshold voltage versus supply voltage, such as the one in **Figure 2**. By fitting a parabola or a polynomial to the experimentally obtained points—say, some 20 points lying in the supply-voltage range of 2 to 15V—you can estimate the threshold voltage, V_T, for any supply voltage.

This circuit has been built and tested. The online version of this Design Idea includes Octave/Matlab code that you can view at www.edn.com/4368072. **EDN**

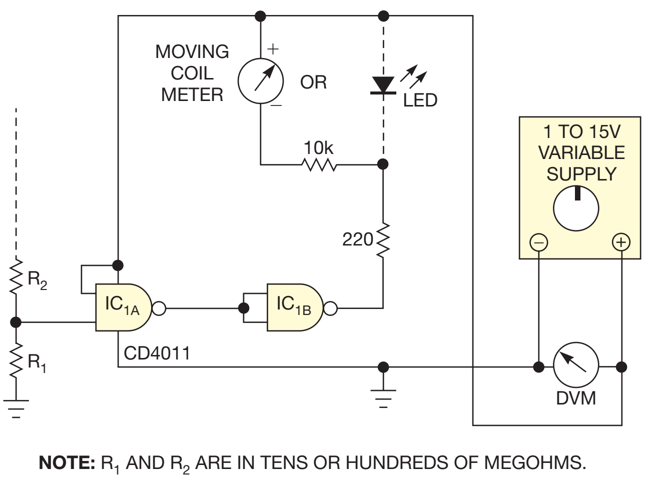

Figure 1 Use CMOS gates and a variable power supply to find an unknown voltage.

Use a photoelectric-FET optocoupler as a linear voltage-controlled potentiometer

Sajjad Haidar, University of British Columbia, Vancouver, BC

You can use a photoelectric FET as a variable resistor or a potentiometer in combination with a fixed resistor. The H11F3M photoelectric FET has an isolation voltage of 7.5 kV, enabling you to safely control high-voltage circuit parameters. The nonlinear-transfer characteristics of these devices are problematic, however (**Figure 1**). To correct the nonlinearity, using a simple feedback mechanism as a potentiometer yields a linear response (**Figure 2**). This circuit uses two photoelectric FETs: one for feedback and the other for applications requiring an isolated potentiometer. You connect the inputs of the two photoelectric FETs in series to ensure the same amount of current for the input LEDs.

Place 50-kΩ resistors at the FET outputs to mimic the response of a potentiometer. The circuit amplifies the difference between the set input voltage, which you adjust using potentiometer R_7, and the feedback from photoelectric FET 1. The resulting output controls the current in the

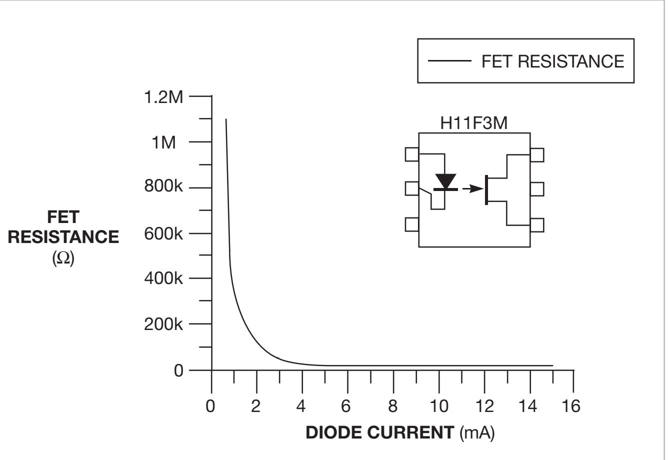

Figure 1 The output resistance of a photoelectric FET is nonlinear with respect to the input-LED current.

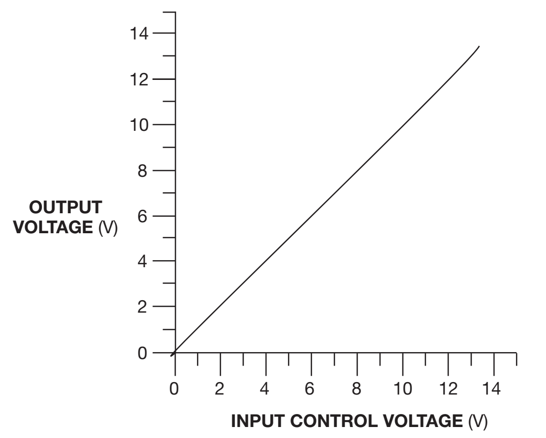

Figure 3 The feedback circuit greatly improves output linearity.

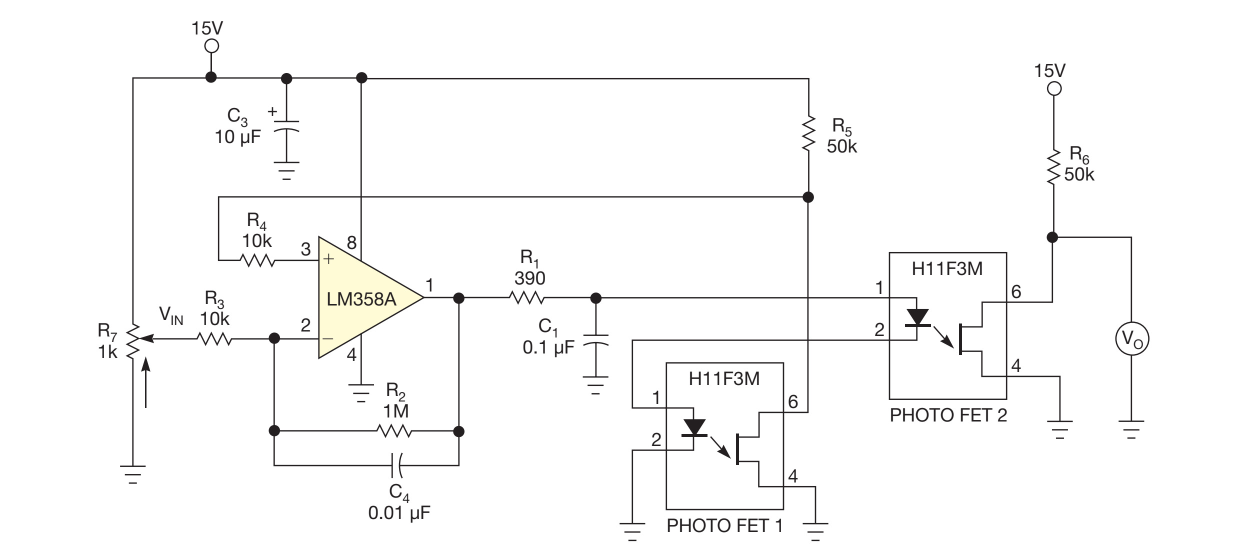

Figure 2 This circuit feeds back the response of an identical photoelectric FET to linearize the response.

photoelectric-FET LEDs until the feedback voltage equals the input voltage. The output voltage follows linearly with the input voltage (**Figure 3**). You might think that photoelectric FETs bearing the same part number are identical, but small manufacturing discrepancies can be present. Five H11F3M parts have offsets within 3%. **EDN**

Minimize noise in power-supply measurements

John Lo Giudice, STMicroelectronics, Schaumburg, IL

You must minimize noise when measuring ripple in power rails because the ripple's amplitude can be low. Oscilloscope probes are essential measurement tools, but they can introduce noise and errors. Ground leads, such as those that attach to standard oscilloscope probes, can add noise that's not present in your circuit to an oscilloscope's trace. The wire loop acts as an antenna that picks up stray magnetic fields. The larger the loop area, the more noise it picks up.

To prove this theory, connect the oscilloscope ground lead to the probe tip and move it around. The oscilloscope will show the noise increasing and decreasing with the ground-lead movement. You can use an oscilloscope probe with its ground lead and sockets to build a simple interconnect board (**Figure 1**).

Start by removing the probe's cover, which reveals the probe tip. There is a short distance between the tip and the ground ring. You need one of two sockets: a right-angle, or horizontal, socket or a vertical socket, similar to those in **Figure 1**.

Solder the center leg of the socket to the output of the power supply, and solder the other leg to the power-supply return. Connect a 0.1-μF surface-mount, stacked ceramic capacitor between the two sockets. This step limits the probe bandwidth to approximately 5 MHz, which further reduces high-frequency noise and lets the lower-frequency ripple pass through. **Figure 2** shows the completed interconnect board; **Figure 3** shows a schematic of the board.

Insert the probe tip into the socket to measure ripple. You will get a ripple measurement without spikes or other noise.

You should use a multilayer stacked ceramic capacitor because it's better at decoupling high-frequency noise. Electrolytic, paper, and plastic-film capacitors comprise two sheets of metal foil with a sheet of dielectric separating the metal sheets, and these three components form a roll. Such a structure has self-inductance; thus, the capacitor acts more like an inductor than a capacitor at frequencies higher than a few megahertz.

Figure 4 shows the impedance to the power supply for various stacked-ceramic-capacitor values. **EDN**

Figure 1 A standard oscilloscope probe has a ground lead that can pick up noise.

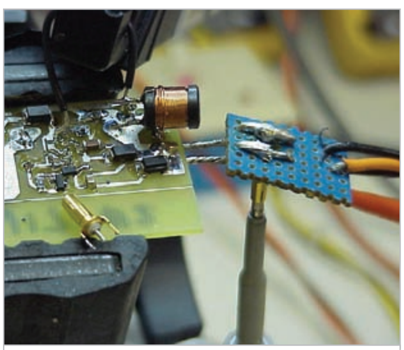

Figure 2 Solder wires from the power supply under test to an interconnect board reduce ground-lead length.

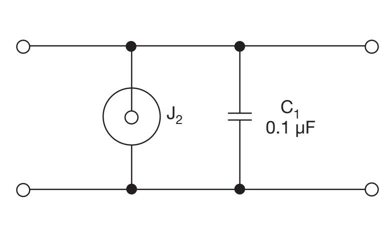

Figure 3 A ceramic capacitor further reduces high-frequency noise.

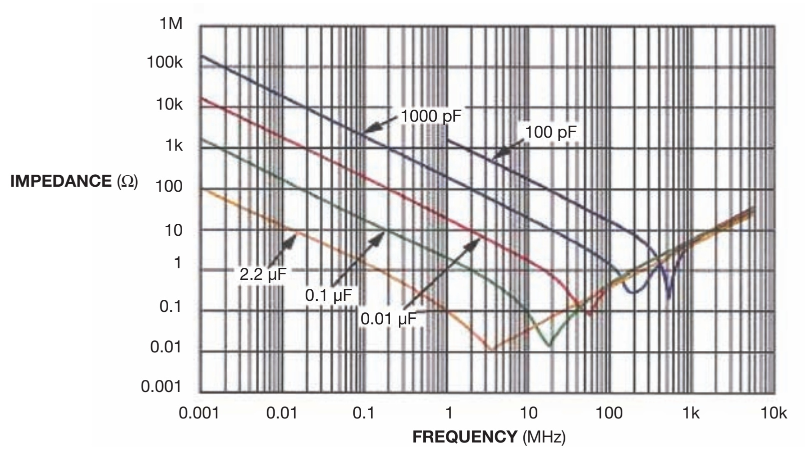

Figure 4 Probe impedance varies with capacitor value.

Probing system lets you test digital ICs

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

This Design Idea describes a simple yet powerful handheld probe that you can use as both a logic probe and a pulse generator either individually or simultaneously. This feature makes the probe useful for testing DIP digital ICs, such as gates, flip-flops, and counters, using a socketed fixture with three-post jumpers to connect each pin to logic high or logic low or to 5V or ground.

Three pushbutton switches, two dual-color LEDs, and two probe tips are built into a plastic cylinder, such as an empty, 20g or larger glue-stick tube. The generator's probe tip hooks to fit onto the test fixture's jumper pins and mounts onto a spring—such as those in retractable ball-point pens—for flexibility, and it allows the logic-probe tip to move to the output under test. Two of the pushbutton switches set the generator's quiescent state for a high or low output. The third switch briefly single-pulses the output to the opposite state. If the switch is pressed for longer than 2 seconds, the output produces a pulse train.

IC_{1A}, an NE556, is a 2-sec monostable circuit, which triggers a 1-msec-pulse generator circuit employing gate G_1, resistor R_1, and capacitor C_1 (**Figure 1a**). G_4 buffers the circuit. The output of the monostable circuit also passes through G_2 and G_3 to mask the output of the astable component, IC_{1B}, an NE556 that provides the pulse train. To prevent any spurious pulse from reaching output Probe A when switch S_1 is not depressed, keep IC_{1B} deactivated by applying a low voltage to its reset pin 4 through transistor Q_1, whose biasing is further guarded by a 0.68-μF capacitor.

When you press switch S_1 for a short

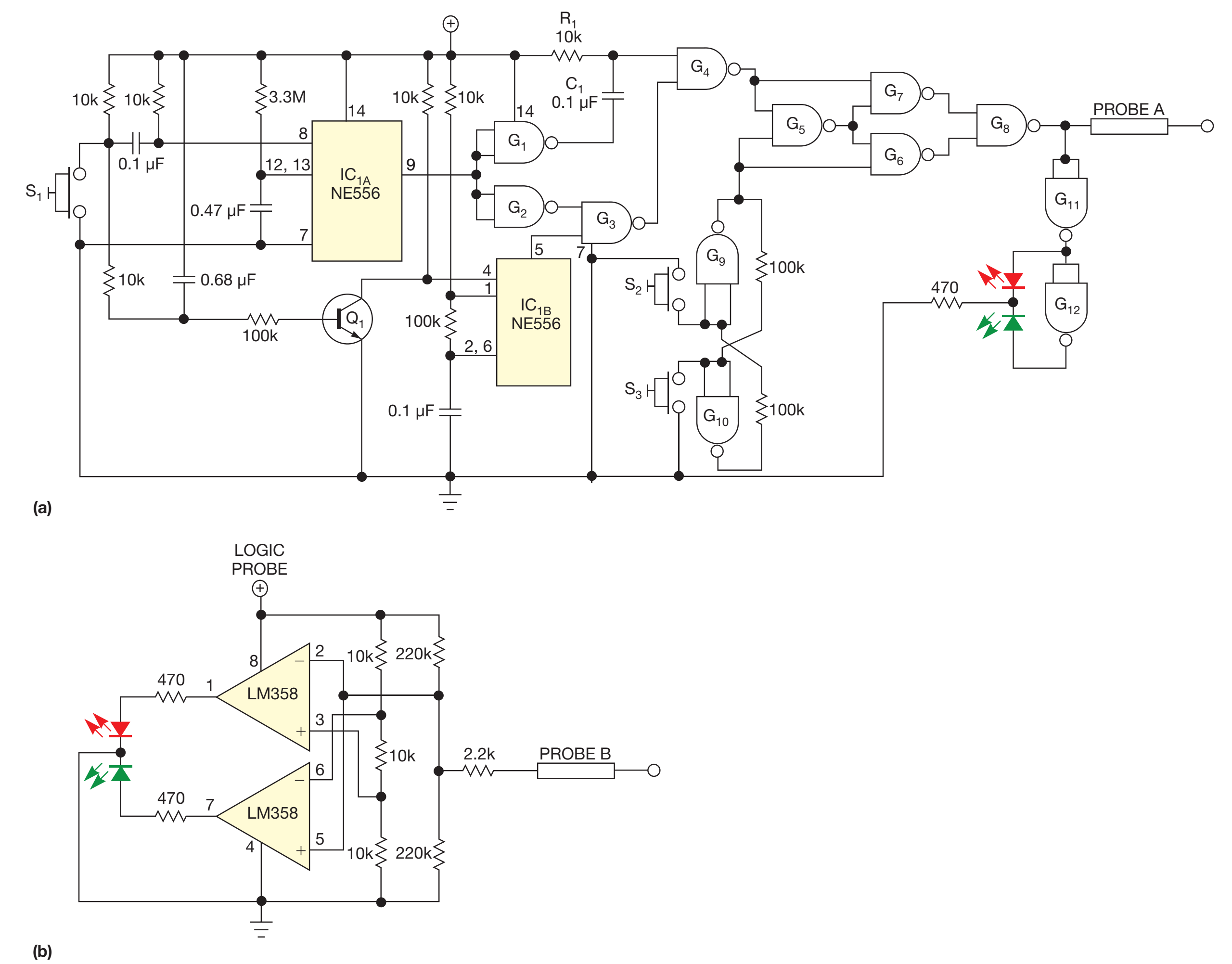

Figure 1 This circuit combines analog and digital functions. Probe A is the pulse-generator probe, and Probe B is the logic probe (a). Although not shown, a 100-μF capacitor should be connected between the supply and ground. Red LEDs indicate logic zero, and green LEDs display logic one (b).

time, IC_{1A} fires and produces a high output for approximately 2 sec. The 1-msec pulse from G_1, R_1, C_1, and G_4 reaches the pulse Probe A through the XOR function comprising G_5 through G_8, and the output of the astable IC_{1B} is masked at G_3 from reaching the XOR. If you depress switch S_1 for longer than 2 sec, the monostable IC_{1A} times out. This action unmasks G_3 and allows the 70-Hz oscillation from IC_{1B} to reach the XOR.

G_9 and G_{10} form a bistable circuit, which "remembers" the most recently pressed S_2 or S_3 switch and controls the inverting and noninverting operation of the XOR function. G_{11} and G_{12} together drive the dual-color LED to indicate the pulse generator's polarity. Red indicates that Probe A's output is mainly logic zero, with the single 1-msec pulse a logic high. Green indicates the opposite.

The LM358 acts as a window-detector logic probe (**Figure 1b**). With the values in the **figure**, the red LED lights at Probe B voltages of less than 35% of the supply voltage, and the green LED lights at voltages greater than 65% of the supply voltage. Neither LED lights between these voltages. You may wish to adjust the resistor network to reduce the lower threshold to include the transistor-transistor-logic zero of less than 0.8V.

If you use CD4011 quad NAND gates, you can externally power the probe at 4.5 to 15V. Using a CD4093 Schmitt-trigger quad NAND for G_1 through G_4 ensures no spurious oscillations as a result of the slow voltage rise at timing capacitor C_1. If your design requires a higher-current generator drive, you can add a pair of NPN and PNP boost transistors to the output.

Figure 2 shows a jig for testing the digital ICs. Configure the 16-pin DIP socket for the device under test with an array of triple-post headers and push-on jumpers. You can connect any pin directly or through a resistor to power or ground to configure power or logic levels. The resistors can be any suitable value; approximately 2 kΩ is appropriate.

To set a TTL low, the pin must connect directly to ground. To inject a signal, hook the flexible spring-mounted generator, Probe A (**Figure 3**), onto the appropriate input post and move logic Probe B to the corresponding output post or pin. See a suggested perf-board layout at www.edn.com/4374947.EDN

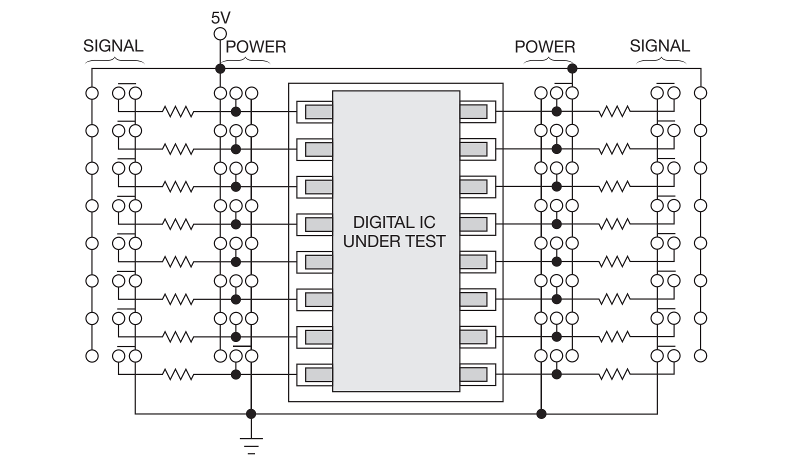

Figure 2 Program this test jig with header posts and jumpers for the IC under test.

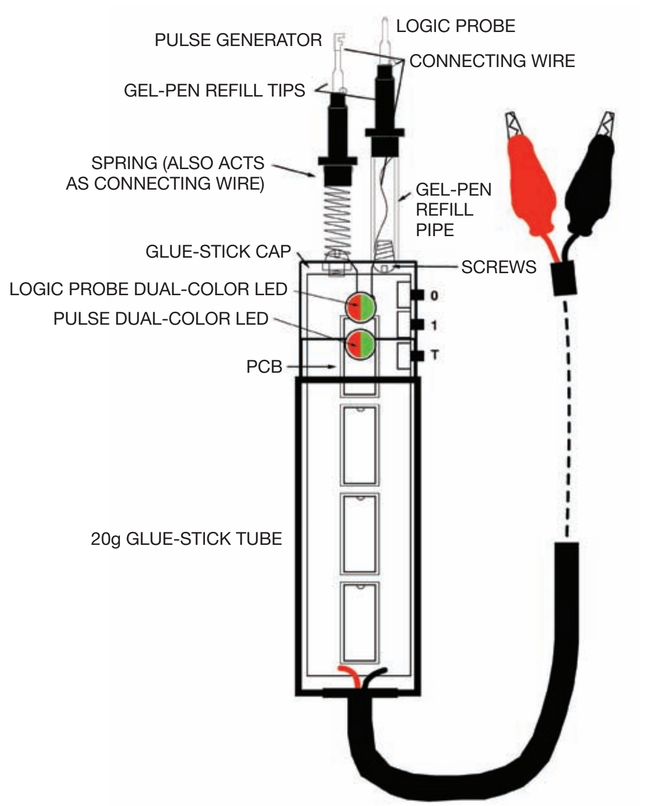

Figure 3 To inject a signal, hook the flexible spring-mounted generator, Probe A, onto the appropriate input post and then move logic Probe B to the corresponding output post or pin.

REFERENCES

1 Baddi, Raju, "Logic probe uses six transistors," *EDN*, Dec 15, 2010, pg 46, http://bit.ly/n24oau.

2 Rentyuk, Vladimir, "Logic probe uses two comparators," *EDN*, Aug 25, 2011, pg 54, http://bit.ly/wtuKgi.

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